AN10829

SSL2101 dimmable high efficiency flyback design

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Document information

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Abstract	This application note describes a simple and highly efficient flyback converter application design for low output power.

Revision history

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v.3	20110622	Modifications: • Text updated • Template upgraded to latest version • All illustrations upgraded to new quality standards • Section 6 “Legal information” amended to include new items
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1. Introduction

The SSL2101 IC is designed for controlling mains dimmable LEDs. This application note describes a design for a simple and highly efficient flyback converter application for low output power.

1.1 Application requirements

The application described in this note is a retrofit application using a lamp within the existing infrastructure. It targets the lower end of the market, which has the following requirements:

- The lamp should be inexpensive.
- The lamp should be compact as the space in the pre-designed housing is limited. The maximum input power for this housing is 7 W.
- The driver should have a high efficiency with a target of 75 %.
- The lamp should be compatible with a triac dimmer, without noticeable flicker or jumps on the output. Transistor dimmer compatibility is optional.
- The input voltage is 230 V, 50 Hz.

1.2 Design choices

The application requirements result in the following design decisions:

- To meet the low power and small form-factor requirements, the design will be based on the SSL2101 IC.
- To meet the 7 W input and 75 % efficiency target, 4 white LEDs are chosen that are in series at the output and supplied with 400 mA current.
- A flyback converter design is used. Using a Schottky diode as a flyback diode will increase efficiency when compared to a Buck design. An additional advantage is the electrical isolation of the LEDs from the mains supply, which means that a metal heat sink can be used to cool the LEDs.
- To improve efficiency, a third winding is used to generate V_{CC} and also to detect any demagnetization of the transformer. This allows the application to run in Boundary Conduction Mode, with low peak current through the transformer.
- The choice was made to only support triac dimmers as they require less components whereas transistor dimmers require their internal power generation to be fed, which reduces the efficiency of the application.

1.3 SSL2101 IC

The SSL2101 is essentially a switch mode power supply controller IC, based on the NXP STARplug series. Additional features are added to give the chip its primary function, a mains dimmable LED driver. Among these functions are the following:

- A logarithmic response at the control pin for the oscillator frequency. This gives dimming LEDs a response comparable to dimming incandescent lighting.
- A current sensing pin to detect when the total application current is about to drop below the level required to keep the dimmer functioning correctly. This can then be used to switch on a resistive bleeder to maintain the current.
- Two switches which control the bleeder circuit. This circuit is used to enable the dimmer to drive low-power applications.

A block diagram of the IC is shown in Figure 1. The design decisions lead to the method in which these functionalities will be used. This is explained in Section 2.

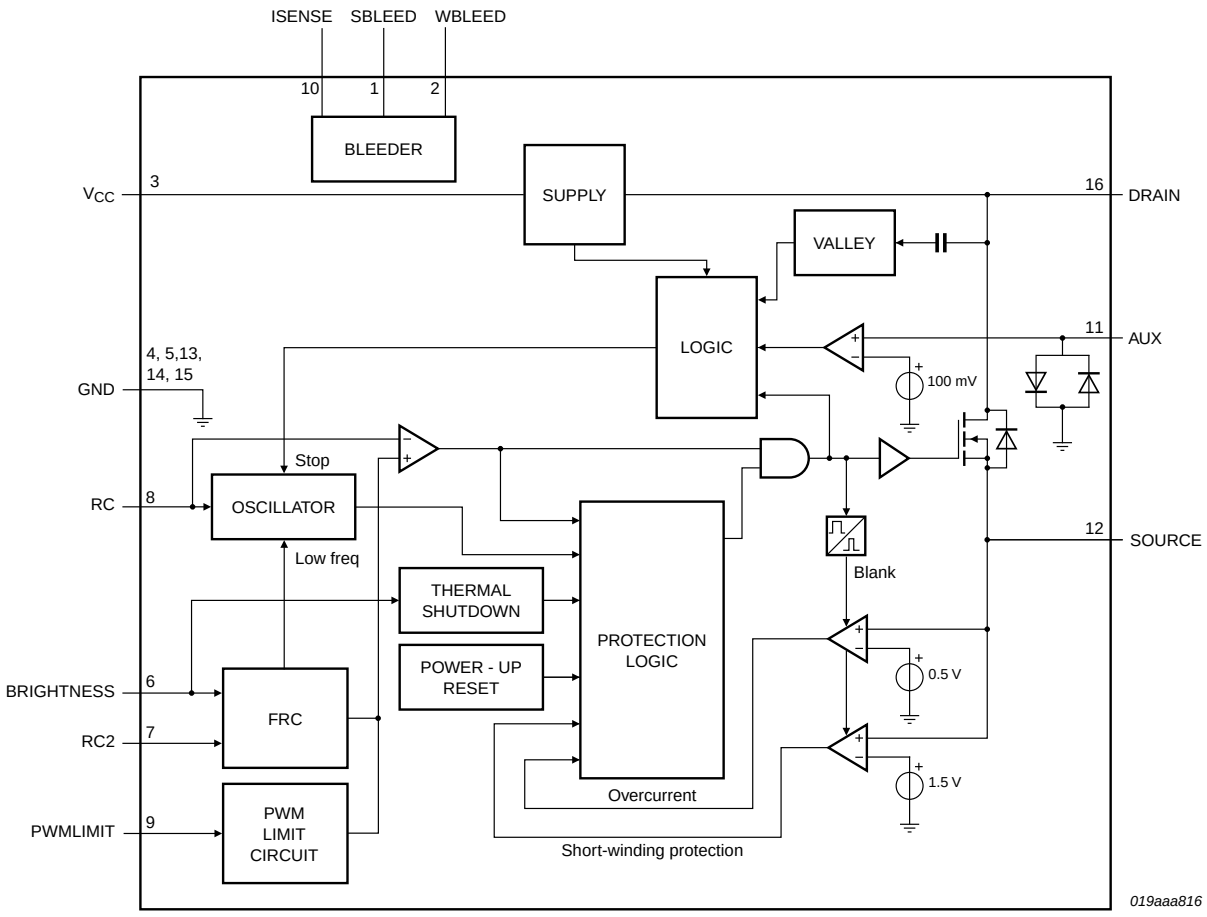

Fig 1. Block diagram of the SSL2101

For more information on the SSL2101, data sheets and application notes can be found on the NXP web site.

2. Designing the application

The application is designed with the choices defined in Section 1.2. This chapter divides the application into its component parts. The following sub-sections discuss the selection of components for these parts. The circuit schematic is shown in Figure 2.

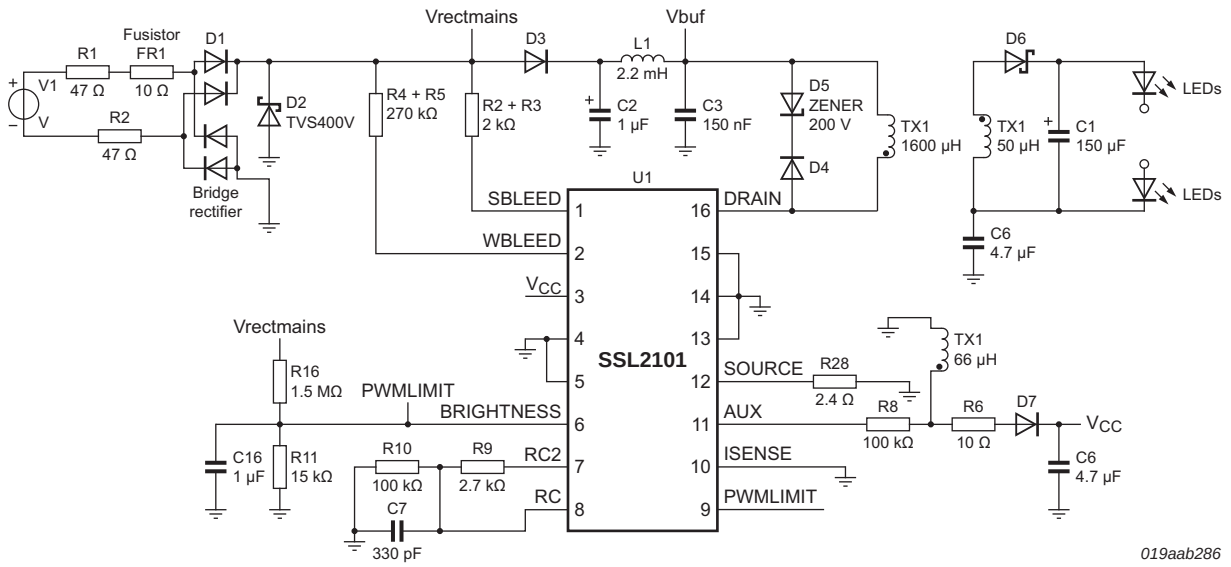

Fig 2. SSL2101 flyback circuit schematic (230 V triac only)

2.1 Switched Mode Power Supply (SMPS)

In low power applications, dimensioning the SMPS plays both an important part for both efficiency and dimmer performance. The requirement for a low cost, small form-factor application further limits the choices for components.

The single-stage convertor consists of two parts, shown in Figure 3.

- An AC-to-DC converter, consisting of a bridge rectifier and a capacitive buffer.
- A flyback DC-to-DC converter, consisting of a transformer with a switched primary side and a secondary with a flyback diode and buffer capacitor.

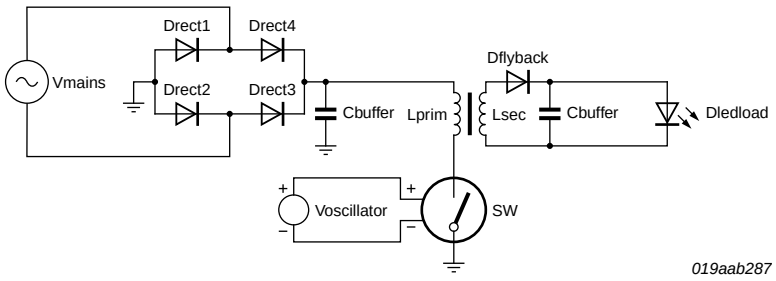

Fig 3. Basic flyback converter

High efficiency requires the converter to run in Boundary Conduction Mode (BCM). When using Discontinuous Conduction Mode (DCM), the peak current through the switch and transformer have to be larger for the same output power. This results in higher resistive losses and it requires a transformer with a larger I_{sat}. Alternatively, running in Continuous Conduction Mode (CCM), the dissipation in the switch increases due to switching losses. The switch used by the SSL2101 is not suitable for this mode of operation.

Choosing BCM adds to the complexity of the application. Additional circuitry is required to detect the boundary between CCM and DCM. The SSL2101 has a special input which can be used to detect the demagnetization of the transformer core. This input is labeled “AUX” because this detection can be done using an auxiliary winding on the transformer.

2.1.1 SSL2101 flyback converter operation

Information on the convertor operation can be found in the SSL2101 data sheet and application note.

The actual output power of the convertor is defined by Equation 1, where:

η = converter efficiency

L_p = primary inductance

I_p = primary peak current

f = converter frequency

$$P = \eta \times \frac{1}{2} \times L_P \times I_P{}^2 \times f \quad (1)$$

The required LED power is 5.25 W. The convertor efficiency is estimated at about 81 % for these low-power applications. The other variables will be discussed in separate sections.

2.1.2 Converter frequency

For optimum efficiency, the application will be running in Boundary Conduction Mode (BCM) in undimmed operation. The operating frequency of the convertor is not only determined by the oscillator RC values in this mode; rather the maximum frequency is limited by both peak current detection and demagnetization detection. The point where demagnetization is detected depends on:

- the inductance
- the primary peak current
- the turns ratio
- the ringing frequency of the transformer (due to the way demagnetization is detected, the oscillator is halted until a valley is detected)

A target convertor frequency of 132 kHz is selected for the following reasons:

- a relatively high frequency requires a lower inductance and/or peak current to transfer the same amount of power
- the convertor frequency must remain below 150 kHz as ElectroMagnetic Interference (EMI) regulations are more stringent above that frequency

- the convertor frequency must remain above the audible range even when the frequency reduces while the circuit is being dimmed.

The convertor frequency also effects the efficiency of the converter and the required transformer size. The inductance and peak current are determined to achieve a frequency that provides a good balance of converter efficiency and transformer size.

2.1.3 Primary peak current and primary inductance

The SMPS primary switch is located inside the SSL2101. This selection is made to eliminate the cost of an expensive high voltage low $R_{DS(on)}$ MOSFET. The switch is optimized for the maximum output power of the IC: 12 W for the SSL2101. The switch $R_{DS(on)}$ is typically 6.5 Ω at 25 °C junction temperature (T_j) and 9.0 Ω at 100 °C (T_j).

The peak current through the inductor is very important. A high current causes high switching losses inside of the IC. As a result T_j rises, the $R_{DS(on)}$ increases and the switch losses increase further. The peak current through the inductor depends on:

- the switch on-time
- the primary inductance
- the primary buffer voltage

The SSL2101 detects this peak current by measuring the voltage drop over a shunt resistor on the SOURCE pin. The switch stops conducting 160 ns (typical) after the voltage level at the SOURCE pin crosses the 0.5 V threshold. This delay causes a higher actual peak current, especially with a high buffer voltage.

A source resistor of 2.4 Ω is used in the circuit which together with the delay and input voltage, leads to a maximum peak current of 0.26 A through the inductor. The primary inductance can be calculated with Equation 2, resulting from Equation 1.

$$L_p = [2 \times P_{in}] / [I_P{}^2 \times f] \quad (2)$$

Using the values mentioned in this section will result in a required primary inductance of 1.6 mH.

2.1.4 Turns ratio

A relatively high percentage of the power can be lost in the flyback diode, due to a low output voltage in relation to the diode forward voltage. A Schottky diode has a lower forward bias voltage that would provide higher efficiency. However, high voltage Schottky diodes have a relatively large forward bias voltage. Increasing the transformer ratio reduces the secondary reverse voltage.

The maximum turns ratio is limited by the minimum buffer voltage, the maximum switch voltage and the required output voltage. For this application, the output voltage is determined by the number of LEDs in series, the current through the LEDs, and the forward voltage over the flyback diode. The estimated required output voltage is 13.2 V. It is estimated that the buffer voltage on the primary side can go as low as 80 V as a result of the buffer capacitance, the load and the sinusoidal mains voltage. Consequently, the winding ratio must be smaller than 6.06 : 1 to be able to generate a constant output voltage, and a turns ratio of 6 : 1 is selected. This results in a maximum reverse voltage of 67 V on the flyback diode.

The transformer specification is discussed in Section 2.1.6. Details relating to oscillator frequency and duty-factor modification to achieve dimming can be found in Section 2.5.

2.1.5 V_{CC} generation

The SSL2101 has an integrated voltage regulator that generates the 5 V supply voltage (V_{CC}) required to drive the logic and the switches. This regulator is either powered from the V_{CC} pin or from the DRAIN pin and switching between the two is done internally.

The regulator is usually powered by the DRAIN pin voltage during startup. However, if the V_{CC} is powered from the DRAIN pin during normal operation, approximately 600 mW is dissipated in the IC: This reduces the application efficiency and possibly the lifetime of the IC. It is advisable to feed the V_{CC} regulator from the V_{CC} pin during normal operation. The voltage on the V_{CC} pin should be between 10.75 V and 40 V. From an efficiency perspective, it is beneficial to keep the V_{CC} voltage low to minimize the regulator dissipation.

In this high efficiency design, the auxiliary winding is used to generate V_{CC}. During a second stroke, the maximum voltage on the secondary winding is limited by the voltage on the output buffer capacitor. Furthermore, the V_{CC} buffer voltage is equal to the output voltage multiplied by the turns ratio between the secondary and auxiliary windings. Four white LEDs are placed in series, which results in a total forward voltage of 12.5 V. This is already sufficient for the V_{CC} pin. For safety reasons, the output is isolated from the input, so V_{CC} cannot be drawn from the output buffer. A diode-capacitor buffer similar to the output buffer is placed on the auxiliary winding to generate the V_{CC} supply.

The exact number of turns on the auxiliary winding is not critical for demagnetization detection as long as the minimum voltage requirement is reached. It can be selected for optimal V_{CC} generation. If the auxiliary winding has an equal amount of turns, then V_{CC} would be equal to 13 V when the application is connected to mains. However, the current through the LEDs is reduced when the application is dimmed. This results in a lower forward bias voltage, which could drop below the required 10.75 V minimum startup voltage.

Remark: The voltage on the DRAIN pin can sometimes still take over during deep dimming, as the buffered voltage will be lower. This is not optimal however, and requires the number of auxiliary turns to be increased.

From an efficiency point of view, the number of auxiliary turns should not be much larger than that of the secondary winding, as the difference between the V_{CC} pin voltage and the 5 V V_{CC} is dissipated. A turns ratio of 1 : 1.2 secondary to auxiliary is used. It is still required to have a small 10 Ω resistor in series with the buffer diode, to filter the voltage peak due to leakage induction.

Remark: For detailed information on optimizing the V_{CC} generation circuit, refer to the application note *AN10754*: SSL2101 and SSL2102 dimmable mains LED driver.

2.1.6 Transformer specification

The application design is based around an efficient transformer, the specifications of which are as follows:

- Core size E16/EFD16.
- Primary: 1600 μH, 54 turns, 0.25 mm wire.
- Secondary: 44 μH, 9 turns, 2 × 0.315 mm wire.
- Auxiliary: 54 μH, 10 turns, 0.1 mm wire.

The required transformer air-gap depends on the properties of the core and core material.The magnetic field strength must be calculated and checked with core material properties in order to avoid saturation. To achieve this, the core size and the turns count are balanced. A double secondary wire can be used to reduce both skin-effect and resistive losses. The proximity losses do not increase, because the wires can run next to each other without increasing the layer thickness. To reduce leakage induction, the secondary winding can be sandwiched between two layers of primary windings. Fringing field losses can be reduced by avoiding windings near the air-gap.

2.2 Input and output buffer

The mains AC input is sinusoidal. Once rectified, it still has a zero-cross point where no power is available for the convertor. To bridge the gap, it is required to use a buffer. The total buffer capacitance required for the specified output current ripple can be divided over the input and the output circuit:

- When the primary buffered voltage drops, the current into the inductor rises to keep the power constant. A large primary capacitor results in a small ripple on the primary buffered voltage and thus a lower peak current through the switch and inductor. This will both save space, as a smaller transformer can be used, and increase efficiency as a result of lower resistive losses in the switch and transformer. Unfortunately, a large primary capacitance also results in a lower power factor (~0.7).
- Reducing the primary buffer capacitance improves the power factor. As the capacitance is now used purely to filter the converter currents, the input current follows the rectified mains voltage. The resultant power factor can be in the order of 0.98. However, the output current will also follow the input voltage. This results in a 100 Hz modulation which, when combined with other modulated sources, can become visible and provide a less effective utilization of the attached LEDs. To compensate for this, a large output capacitor must be used to average the current. As a result, the peak current through the inductor will be 41 % or larger, at the rated output, which requires a bigger transformer.

When a triac dimmer is used, sizing the input buffer becomes more complex, as the triac inside the dimmer responds to the current being drawn by the circuit. A triac can be seen as a bidirectional thyristor. This device requires a minimum current to start conducting, or “ignite”, and a minimum current to remain conducting: These are referred to as the “latching current” and the “hold current”.

- When a high primary buffer capacitance is used, the buffered voltage can be higher than the trigger voltage of the triac. This will result in insufficient latching current and the triac will not fully ignite. The triac output voltage will follow the buffered voltage

until the difference between the mains voltage and buffered voltage is again equal to the trigger voltage. At that moment the triac fully ignites and an example of such a situation is provided in Figure 4.

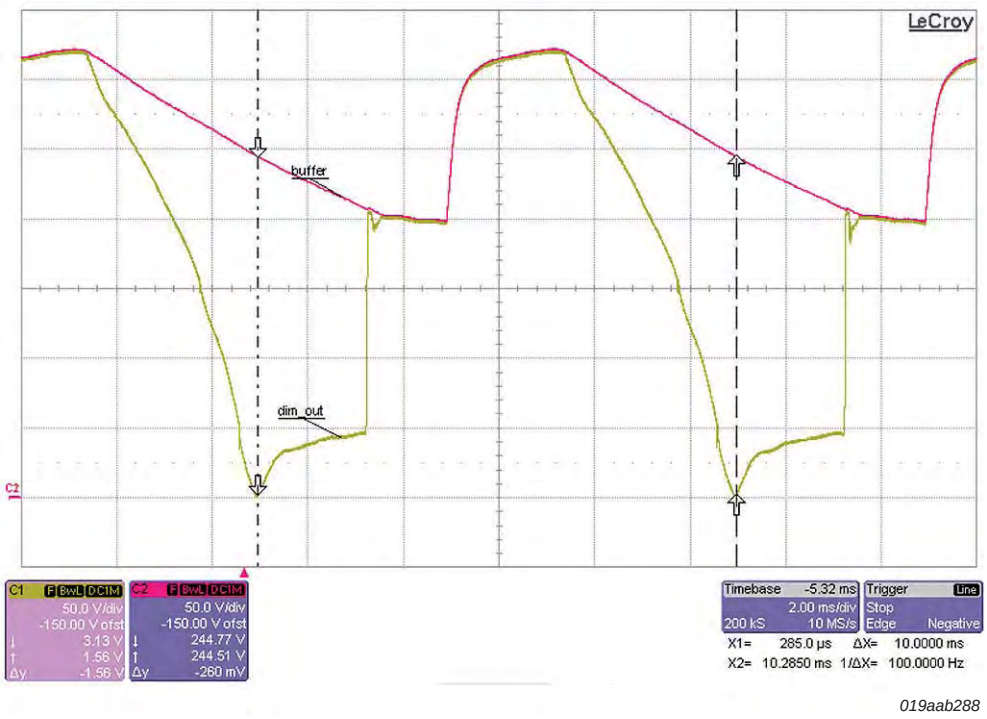

Fig 4. Improper triac latching resulting from a large buffer capacitance

- When a small primary capacitance is used, the buffer is charged by a short current pulse after which the current drops below the minimum hold current and the triac switches off. However, the buffer capacitor is quickly drained and the buffer diode starts conducting again. This results in the triac reigniting, which is also referred to as “multiple firing”. An example of this is provided in Figure 5.

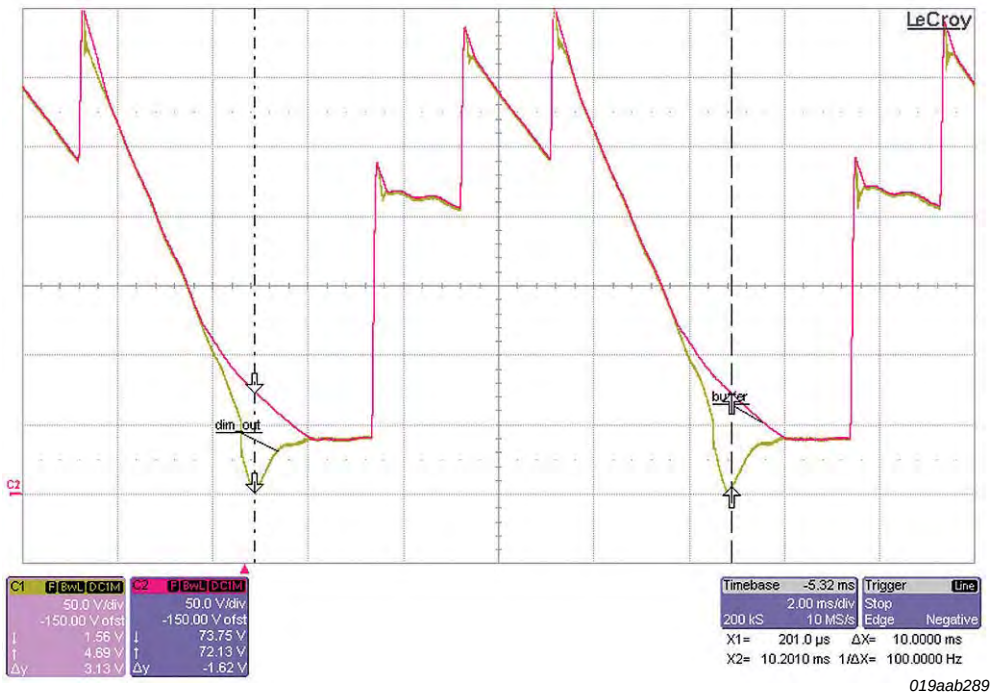

Fig 5. Multiple firing resulting from a small buffer capacitance

In this design the dimmer position is determined by taking the mean value of the rectified input voltage. Both of the above mentioned effects will influence this value. In the best case this results in a step in the output, as a triac goes from normal to abnormal operation. However, this jump could set the triac back to normal operation, which in turn then jumps back to the abnormal mode and so on. This unstable situation results in an oscillation (visible) in the output current, referred to as “flickering”.

Abnormalities in dimmer operation should be avoided as much as possible, to reduce the chance of flickering. To avoid this, the SSL2101 has a bleeder circuit. This is discussed in Section 2.3.

In this design, a 1 µF electrolytic capacitor is combined with a 150 nF (film) capacitor to handle peak currents. This gives a good balance between dimmability and efficiency. However, the value of the damping resistor also plays a large part. This is discussed in Section 2.4. Encapsulated film capacitors are used to reduce audible noise to a minimum.

2.3 Bleeder circuit.

Triac dimmers are designed for high power loads, usually in the order of 40 W to 600 W. All internal circuitry is optimized for these loads. When a load with a lower power rating is connected, the dimmer often behaves abnormally, switching on and off at unpredictable times. Placing a resistive load in parallel to dissipate the minimum required power could remove this problem. But as high efficiency is almost always a target, that would not be an option. This problem can be solved by properly loading the triac dimmer at the right times.

To summarize, the triac requires a minimum current to latch and a minimum current to hold. Additionally, a higher (minimum) current is required to reset the dimmer's internal timing circuit around zero-crossing of the mains voltage.

- In the SSL2101 design, the triac latching current mainly consists of the charging current of the primary buffer capacitor. Because this is finite, the higher the current the shorter the latching time becomes, and vice versa. This current has to be above a certain minimum value. However, in power consumption terms, there is an optimum balance between a low and high current. The strong bleeder can also contribute and this is discussed in Section 2.3.1.
- The minimum hold current that is required, differs between triac types and between dimmer positions. Approximately 20 mA of hold current should be drawn to ensure every triac stays latched in normal operation. However, because the charging of the buffer capacitor usually happens in a single small current pulse, the 20 mA has to be drawn another way. This can be done with a current source or, as is the case for the SSL2101, by switching on a weak bleeder resistor.
- A triac conducts when triggered by a RC-circuit inside the dimmer. The weak bleeder resistor used for the SSL2101 is insufficient to charge this RC-circuit, so for voltages below 54 V, a 2 kΩ strong bleeder resistor takes over.

The SSL2101 circuit includes all the facilities to support triac dimmers. Dimensioning of the buffer was previously discussed in Section 2.2 and the strong bleeder resistor is 2 kΩ for almost every application, however, it is more difficult to select the right value for the weak bleeder resistor. This is discussed in Section 2.3.1.

2.3.1 Dimensioning the weak bleeder resistor

The internal SSL2101 IC switch can handle a maximum current of about 14 mA. For some triac dimmers this is not a sufficient hold current and the dimmer reacts by switching off.

When the triac dimmer switches off, the voltage does not immediately drop to zero; instead the voltage drops slowly. Additionally, when the triac switches off this way, the timing circuit inside the dimmer is not reset properly. Because the timing circuit and the brightness circuit then become mutually dependent, this often results in flickering. An example is shown in Figure 6. The first two phases in Figure 6 show the triac igniting a second time (multiple firing).

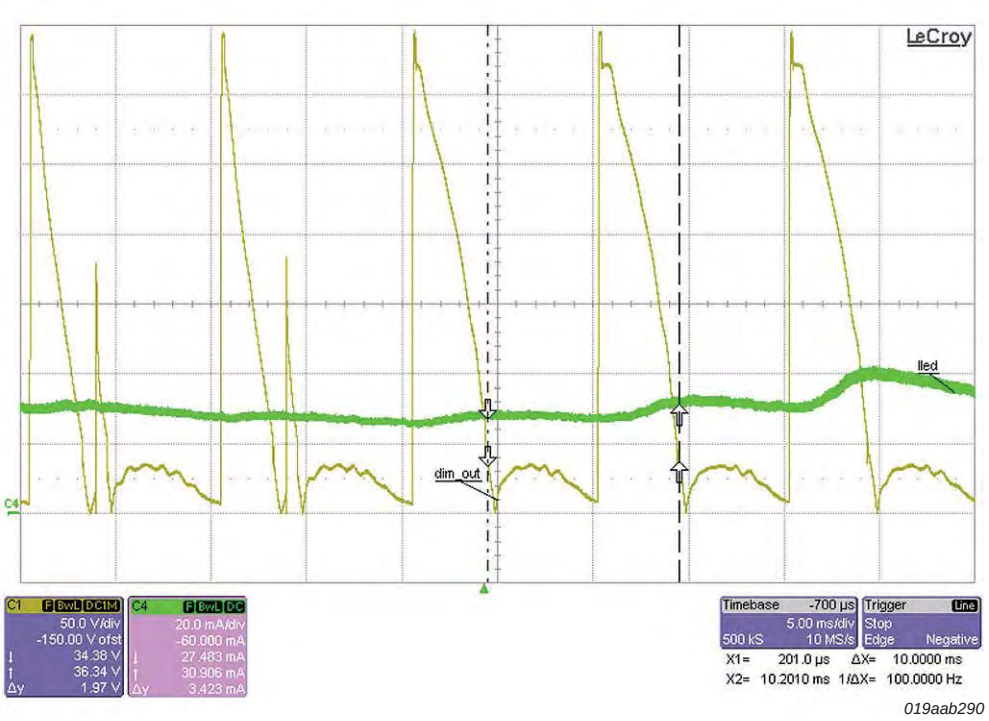

Fig 6. Output current oscillation resulting from insufficient hold current

The hold current can be increased by means of an external transistor, which is controlled by the WBLEED pin. However, to maximize efficiency, another solution is used. The hold current is removed altogether and as a result the triac always switches off in the same predictable way. This results in consistent behavior.

A weak bleeder resistor still has to be present to detect the rectified input voltage level. This reference voltage is used to detect the 54 V switch level for the strong bleeder. If this is not detected, the strong bleeder switch stays on for the whole phase. This could cause damage to both the strong bleeder switch and resistor.

The value of the weak bleeder resistor can be used to control the switching point of the strong bleeder:

- A larger weak bleeder resistor delays the switching moment. If it is too large, the strong bleeder switch and resistor become over-stressed again.
- A smaller weak bleeder resistor advances the switching moment. If it is too small, the unstable situation due to an insufficient hold current, reoccurs (see Figure 6).

In this application, the ISENSE pin is connected to ground, which means the weak bleeder switch is always on (except when the strong bleeder takes over). The selected resistor value is 270 kΩ which provides a good balance between the issues explained above.

2.4 Damper circuit

The damper circuit limits the in-rush current and it damps oscillations due to the inductive and capacitive elements inside the dimmer and the mains network. The in-rush current is a high current peak that occurs on two occasions:

- When the buffer capacitors are not charged and the application is connected to a high voltage source, the current is only limited by the parasitic resistance Equivalent Series Resistance (ESR) of the capacitors. The resultant current peak is very high and could damage components or blow a fuse.
- When the application is connected to a triac dimmer, this peak occurs every phase. However, the dimmer's internal components (a large output inductor and the triac on-resistance) now limit the current.

Because of the importance of low cost and small size in this application, a series damping resistor is chosen to limit the current. The major disadvantage of this damping resistor is that all the current passes through it, resulting in a continuous and unnecessary power loss.

The resistance of a damper is important for dimmability. When the charging current of the primary capacitors is limited, the charging time increases. As a result, the charging current also contributes to the hold current for the triac.

- If the damping resistor is too large, the power loss will be unnecessarily large and it can also cause triac latching issues due to insufficient latching current.
- If the damping resistor is too small, there will be a switch-on oscillation of the current. After an initial peak, the current will reduce shortly to a very low level that can be below the hold current of the triac. The triac will either not latch properly if the peak is too short or it will re-open because the hold current is not present.
- If the damping resistor is too small, the inrush current can become excessive, especially when connected to a triac dimmer with a duty factor just over 50 %. Because the buffer capacitor is only charged during a short current peak, it is not fully charged. Consequently, the triac switches off due to insufficient hold current before the input voltage has finished rising. However, the difference between the mains and buffered voltage is not sufficient for the dimmer to reignite until the end of the cycle. Multiple firing occurs, which can be seen in Figure 7. This figure also shows the moment when the triac latching is again inconsistent, which can result in flickering. The problem increases for larger dimmer duty factors, as can be seen in Figure 8.

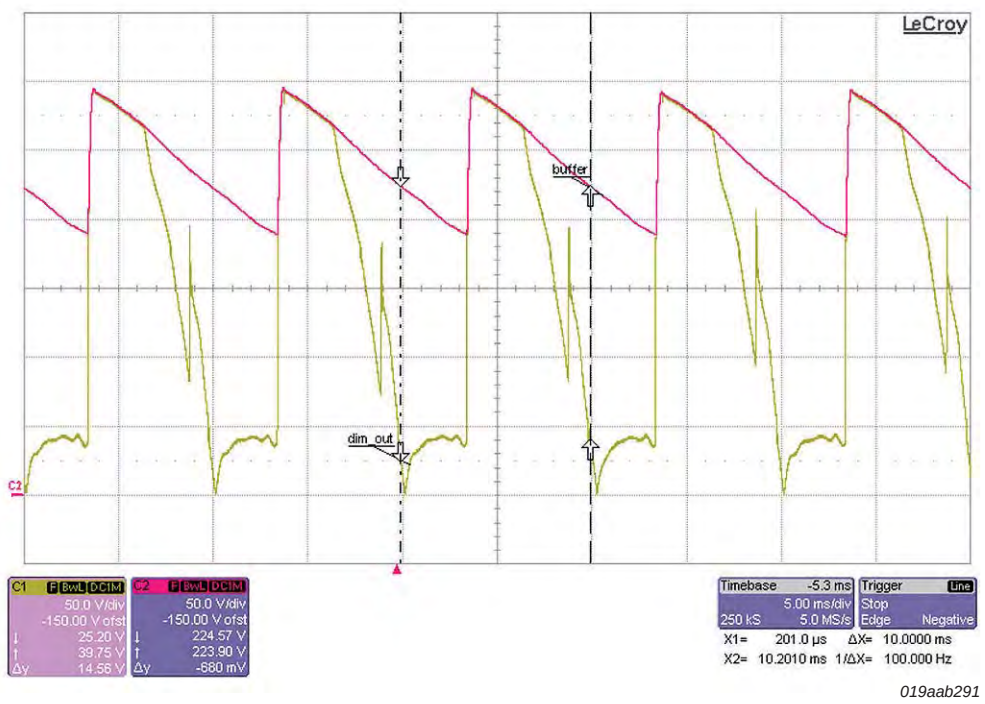

Fig 7. Unpredictable dimmer behavior due to insufficient damping

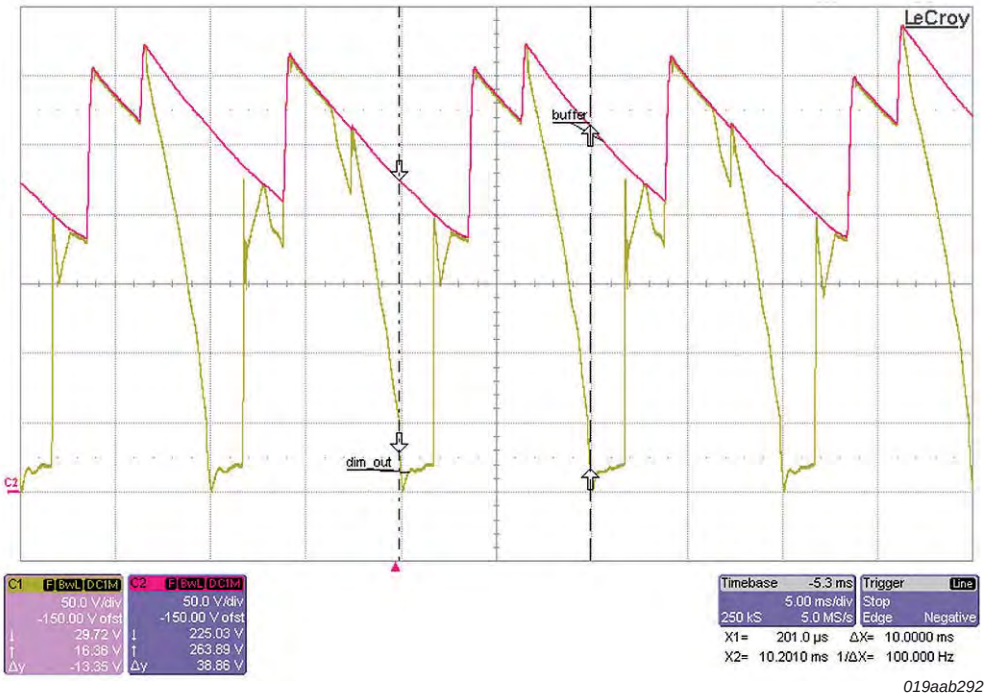

Fig 8. Advanced state of multiple firing due to insufficient damping

The dissipation in the damping resistor is related to the time and amplitude of the inrush current. The inrush current is related to the charge of the input buffer capacitance. Finally, the buffer capacitance is related to the lamp power. Larger lamp powers require a larger capacitor to store sufficient energy.

Because dimmer performance is very important, the value of the damping resistor is optimized for triac dimmers. A single resistor is only feasible for power levels below 12 W. Above this output power, too much power is lost in the damper and other solutions are required. The solutions could be a combination of a serial and a parallel damper or an active damper that bridges the serial damper when the inrush current peak has passed.

For this application a damping resistor value of approximately 100 Ω is selected. This resistor is placed before the rectifier and it is evenly distributed using a 47 Ω resistor in each path.

2.4.1 Active damper

This section describes a low power active damping circuit. Only a small amount of power is lost in the damping resistor. When the output power requirements increase, so does the input current. As stated by Ohm's law, the power lost in the resistor is the square of the current through the resistor divided by its resistance. However, the maximum inrush current will become too large if the value of the resistor is reduced.

An active damper links the resistance of the damper to the current through the application. During normal use with a small current (connected to mains for example), the resistance is low. When a peak current occurs, the resistance is increased. The aim is to limit the current to a maximum value which can be achieved with a current source. An example can be seen in Figure 9.

- The MOSFET is turned on as long as its gate voltage is larger than its source voltage V_{R1} plus the threshold voltage V_t, so that the 100 Ω resistor is bypassed and the 3.3 Ω resistor only is used as a damper.
- The MOSFET exits saturation and turns off when the current increases to the point where the voltage at the source reaches the threshold ($V_{R1} + V_t$) > V1. As a result, the total damping resistance is increased to a maximum of 103.3 Ω (R1 + R2).

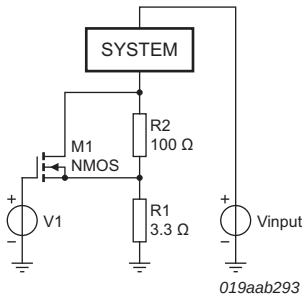

Fig 9. Block diagram for the active damping circuit.

The following extra components, required for the active damper, increase the costs:

- A reference voltage generation circuit, a zener diode for example. This diode can be powered via a resistor from the buffered rectified mains.

- A transistor is required to limit the current. MOSFETs are preferred, but quite expensive. A standard NPN transistor has the problem that it requires a relatively large base current which makes it more difficult to design an efficient reference voltage generator. A Darlington transistor is preferred but a thyristor that resets every phase can also be used.
- The transistor will have to be able to handle a high voltage and considerable power dissipation both of which increase the price and size of the transistor.

2.5 Oscillator and dimming curve

The SSL2101 has multiple inputs that can be used to control the output:

- The BRIGHTNESS pin controls the oscillator frequency. The maximum and minimum frequency is determined by the external resistors and the capacitor connected to the RC and RC2 pins.
- The PWMLIMIT pin controls the duty factor of the oscillator. The maximum duty factor is 75 %.
- The voltage on the SOURCE pin is used to limit the maximum current through the inductor. The switch is opened when the pin reaches a threshold level of 0.52 V.
- The AUX pin can be used to detect demagnetization of the inductor. The oscillator is halted as long as the pin voltage is higher than 100 mV.

The human eye interprets light intensity in a logarithmic way. The light intensity has to be reduced by approximately 80 % for the eye to see it as half the previous brightness. The SSL2101 has an internal brightness curve circuit that compensates for this. This curve is shown in Figure 10.

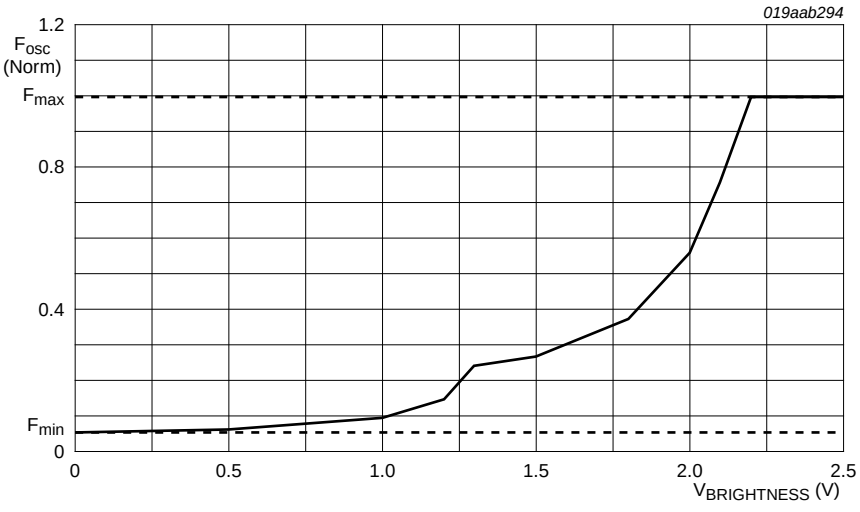

Fig 10. Brightness curve

The brightness curve is created using two logarithmic curves. The transition between the curves can be noticeable when the output is only controlled by the brightness voltage. The output current never reaches zero when the brightness voltage is reduced, so the lamp remains on.

The PWMLIMIT pin is another input that is mainly used for output current control. The PWMLIMIT does not have a logarithmic dimming curve, so the switch close time reacts linearly to changes in PWMLIMIT voltage. As a result, the output power increases squarely with a flyback topology or proportionally with a buck topology.

A fully logarithmic dimming curve that goes from 0 % to 100 % can be made by combining the PWMLIMIT and BRIGHTNESS voltage. The most important factor in determining the correct combination is the value of the RC components. The convertor switch on-time, controlled by the PWM limit, is not proportional to the frequency. When the frequency is increased, the PWM limit curve becomes much steeper.

When the RC values are set by a 330 pF capacitor and a 100 kΩ resistor for the lower frequency, and a 2.7 kΩ resistor for the higher frequency, the PWMLIMIT and BRIGHTNESS pins can be connected together to create an acceptable logarithmic dimming curve. The resultant curve can be seen in Figure 11. When the input exceeds 1.7 V, the output current is clipped by the I_{peak} limit and demagnetization detection.

As a result, the circuit required to control the pins can be minimal with a cost-effective voltage divider for the rectified input voltage.

- A 15 kΩ resistor to ground is selected to generate an offset voltage. Both pins have an internal 20 μA current source, which result in a 0.6 V voltage drop over the resistor. A 1 μF capacitor in parallel to this resistor is sufficient to average the input voltage. Choosing a value that is too large, will result in a slow dimmer response.
- A 1.5 MΩ resistor from the rectified input voltage gives the correct voltage range for the pins connected to mains voltage. This means that the control voltage is already in the clipping range. This is required to compensate for the lower maximum average voltage when the dimmer is supplied via a dimmer instead of being connected directly to the mains.

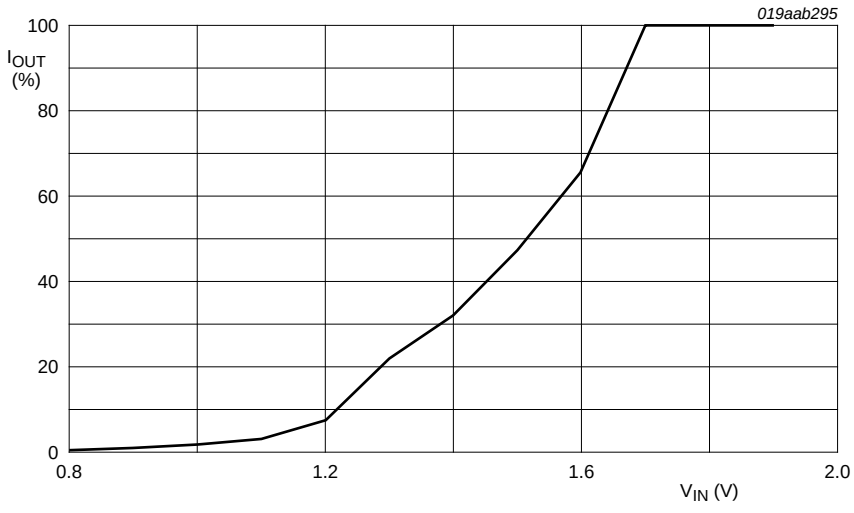

Fig 11. The combined BRIGHTNESS/PWMLIMIT curve

It is very important that the control signal PCB tracks do not pick up any noise from the high power tracks on the PCB. Even small voltage variations can be noticed on the output, especially in the steep part of the curve. This has to be taken into account when laying out the PCB. A small capacitor (~100 pF) can be placed near the input pins for extra filtering.

3. Circuit performance

3.1 Measurement results

The circuit is based on the SSL2101 flyback reference design that is modified to represent the schematic shown in Figure 2.

The board is attached to 4 LEDs connected in series to the output and to the 230 V, 50 Hz mains on the input. The following input and output parameters are compared:

- input voltage - 230 V RMS
- input current - 43.9 mA RMS
- input real power - 6.87 W
- input apparent power - 10.1 VA
- input power factor - 0.693
- output voltage - 12.5 V RMS
- output current - 431 mA RMS
- output power - 5.37 W (power factor ~1)
- efficiency - 78 %

The target and efficiency requirements are met and exceeded. The quality of the transformer and Schottky diode play an important factor in this achievement.

Dimmer performance is an important requirement for the application. No oscillations were observed on the eight dimmers that were tested which are listed in the first column of Table 1. The numbers in the table show the minimum and maximum output currents in mA. Dividing the two values produces the dimming ratio.

Remark: All the dimmers listed are leading edge triac dimmers. For transistor dimmers other circuitry is required

Table 1. Triac dimming ratio for multiple dimmers

Dimmer	I_{min} (mA)	I_{max} (mA)	Ratio
Opus 852.390	7.0	421	1 : 60
Opus 852.392	4.8	425	1 : 89
Busch 2250 U	3.0	418	1 : 139
Busch 2247 U	3.3	427	1 : 129
Gira 1184 00/I00	14.2	427	1 : 30
Everflourish EFO700DA	8.9	427	1 : 48
be T39.01	0.0	421	1 : infinity
drespa primär 815	15.7	423	1 : 27

3.2 Circuit issues

The selection of the primary buffer capacity is based on a balance between dimmability and efficiency. However, some triac dimmers will not fully latch for very high dimmer duty factors. The latching current is not sufficient, as described in Section 2.2, and it results in the situation shown in Figure 4.

One solution to increase the latching current, is to add an RC damper/bleeder on the input (before the rectifier). The capacitor draws an additional current peak for triac ignition, limited by the series resistor. This solution has two main disadvantages, two extra high voltage components are required and power is lost in the resistor. For this reason it is not used in this application.

The issue is solved by changing the dimming curve. The improper latching current has little effect on the buffered mains voltage. Once the triac is properly latched, the buffered voltage goes to the same maximum value of the mains. The jump is caused by a drop in the average voltage, which is used to determine the brightness and PWM duty factor upper limit. As this issue only occurs with high dimmer duty factors, these values are already at, or above, their maximum. In this application, the dim curve is shifted to resolve this issue. Consequently, the brightness and PWM limit voltage values are out of their control range. In this way, the frequency and duty factor limits do not change due to the jump and the output stays the same.

4. Conclusion

This document discussed a design for a 7 W SSL2101 application. The design is based on application requirements which include a 7 W maximum input power, a minimum of 75 % efficiency and low cost. A flyback topology running in Boundary Conduction Mode was chosen. The design choices that were made to achieve the target requirements are explained, including several issues regarding triac dimmer operation. The resultant design offers a 78 % efficiency rating, while maintaining dimmer compatibility at power levels below the dimmer rating.

5. References

[1] AN10754 - SSL2101 and SSL2102 dimmable mains LED driver

[2] UM10341 - SSL2101 12W mains dimmable LED driver

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7. Contents

1 Introduction 3
1.1 Application requirements 3
1.2 Design choices 3
1.3 SSL2101 IC 4
2 Designing the application 5
2.1 Switched Mode Power Supply (SMPS) 5
2.1.1 SSL2101 flyback converter operation 6
2.1.2 Converter frequency 6
2.1.3 Primary peak current and primary inductance . 7
2.1.4 Turns ratio 7
2.1.5 V_{CC} generation 8
2.1.6 Transformer specification 9
2.2 Input and output buffer 9
2.3 Bleeder circuit 11
2.3.1 Dimensioning the weak bleeder resistor 12
2.4 Damper circuit 14
2.4.1 Active damper 16
2.5 Oscillator and dimming curve 17
3 Circuit performance 19
3.1 Measurement results 19
3.2 Circuit issues 19
4 Conclusion 20
5 References 20
6 Legal information 21
6.1 Definitions 21
6.2 Disclaimers 21
6.3 Trademarks 21
7 Contents 22

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